IN THE CLAIMS:

Please amend the claims as follows:

1. (currently amended) An input processing device for use in a re-multiplexing module that processes input packet data, comprising:

an input interface that receives a plurality of data transport streams each of which contains ~~the~~ input packet data;

a corresponding plurality of ~~an~~ input processors coupled to the input interface to receive input packet data from a respective data transport stream ~~therefrom and write data to a packet buffer~~; and

a corresponding plurality of packet identifier tables each of which is coupled to a respective ~~the~~ input processor.

2. (currently amended) An input processing device for use in a re-multiplexing module that processes input packet data, comprising:

an input interface that receives the input packet data;

an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer; and

a packet identifier table coupled to the input processor;

~~The input processing device of claim 1,~~ wherein the input processor includes a serial-to-parallel converter for converting the input packet data received from the input interface.

3. (currently amended) The input processing device of claim 1, wherein ~~the~~ each input processor includes a input processor control logic portion that validates the input packet data.

4. (currently amended) The input processing device of claim 3, wherein ~~the~~ each input processor control logic portion validates the input packet data by extracting a packet identifier number from a header in the input packet data and checking the packet identifier number with the corresponding packet identifier table.

5. (currently amended) The input processing device of claim 1, wherein ~~the~~ each input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field.

6. (currently amended) The input processing device of claim 1, wherein ~~the~~ each input processor includes a data delay register that delays the input packet data before the input processor writes data to ~~the~~ a packet buffer.

7. (currently amended) An input processing device for use in a re-multiplexing module that processes input packet data, comprising:

an input interface that receives the input packet data;

an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer; and

a packet identifier table coupled to the input processor;

~~The input processing device of claim 1,~~ wherein the input processor includes a time reference generator that generates timestamp values for the input packet data.

8. (currently amended) The input processing device of claim 1, wherein ~~the~~ each input processor includes a host processor interface.

9. (currently amended) The input processing device of claim 1, wherein at least one of the input processors is a field programmable gate array.

10. (currently amended) An input processing device for use in a re-multiplexing module that processes input packet data, comprising:

an input interface that receives the input packet data;

an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer; and

a packet identifier table coupled to the input processor;

~~The input processing device of claim 1,~~ wherein the packet identifier table is divided into an active table containing values used by the input processor to select packets for storage in a input packet data stream and a pending table containing values that can be modified by the host processor while the active table is being used by the active table.

11. (original) An input processing device for use in a re-multiplexing module that processes input packet data, comprising:

an input interface that receives the input packet data;

an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer, the input processor including

a serial-to-parallel converter for converting the input packet data received from the input interface;

an input processor control logic portion that receives data from the serial-to-parallel converter;

a program clock reference detector that checks the input packet data for a valid program clock reference field;

a data delay register that delays the input packet data before the input processor writes data to the packet buffer;

a time reference generator that generates timestamp values for the input packet data; and

a host processor interface; and

a packet identifier table coupled to the input processor.

12. (original) The input processing device of claim 11, wherein the input processor is a field programmable gate array.

13. (original) The input processing device of claim 11, wherein the packet identifier table is divided into an active table containing values used by the input processor to select packets for storage in a input packet data stream and a pending table containing values that can be modified by the host processor while the active table is being used by the active table.

14. (original) The input processing device of claim 11, wherein the input packet data includes a plurality of packets, and wherein the input processor control logic portion validates the input packet data by extracting a packet identifier number from a header in a packet and checking the packet identifier number with the packet identifier table.

15. (original) The input processing device of claim 11, wherein the input packet data includes a plurality of packets, and wherein the timestamp value generated by the time reference generator corresponds to a time period during which a packet passes through the re-multiplexing module.

16. (new) The input processing device of claim 1, wherein each input processor checks a length of each packet of said packet data received and discards packets of incorrect length.

17. (new) The input processing device of claim 16, wherein, if an input processor discards a packet of incorrect length, an error bit is set that is readable by a host processor and indicates a packet of incorrect length was discarded.

18. (new) The input processing device of claim 1, further comprising a corresponding plurality of packet buffers, wherein each input processor writes packets of packet data to a corresponding packet buffer if that packet has an identifier that matches an entry in the corresponding packet identifier table.

19. (new) The input processing device of claim 1, wherein each of said packet identifier tables list packet identifiers for packets of data which are to be given priority and be processed before non-priority packets of data.

20. (new) The input processing device of claim 2, wherein the input processor includes a input processor control logic portion that validates the input packet data using said packet identifier table.

21. (new) The input processing device of claim 2, wherein the input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field.

22. (new) The input processing device of claim 21, wherein said input processor flags packets of data that include a valid program clock reference field.

23. (new) The input processing device of claim 2, wherein the input processor includes a data delay register that delays the input packet data before the input processor writes data to a packet buffer.

24. (new) The input processing device of claim 2, wherein the input processor includes a host processor interface.

25. (new) The input processing device of claim 2, wherein the input processor is a field programmable gate array.

26. (new) The input processing device of claim 2, wherein the input processor checks a length of each packet of said packet data received and discards packets of incorrect length.

27. (new) The input processing device of claim 26, wherein, if the input processor discards a packet of incorrect length, an error bit is set that is readable by a host processor and indicates that a packet of incorrect length was discarded.

28. (new) The input processing device of claim 2, wherein said packet identifier table lists packet identifiers for packets of data which are to be given priority and be processed before other, non-priority packets of data.

29. (new) The input processing device of claim 2, wherein the input processor accepts or discards input packet data using said packet identifier table.

30. (new) The input processing device of claim 7, wherein the input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field.

31. (new) The input processing device of claim 30, wherein said input processor flags packets of data that include a valid program clock reference field.

32. (new) The input processing device of claim 7, wherein the input processor includes a data delay register that delays the input packet data before the input processor writes data to a packet buffer.

33. (new) The input processing device of claim 7, wherein the input processor includes a host processor interface.

34. (new) The input processing device of claim 7, wherein the input processor checks a length of each packet of said packet data received and discards packets of incorrect length.

35. (new) The input processing device of claim 34, wherein, if the input processor discards a packet of incorrect length, an error bit is set that is readable by a host processor and indicates that a packet of incorrect length was discarded.

36. (new) The input processing device of claim 7, wherein said packet identifier table lists packet identifiers for packets of data which are to be given priority and be processed before other, non-priority packets of data.

37. (new) The input processing device of claim 7, wherein the input processor accepts or discards input packet data using said packet identifier table.

38. (new) The input processing device of claim 10, wherein the input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field.

39. (new) The input processing device of claim 38, wherein said input processor flags packets of data that include a valid program clock reference field.

40. (new) The input processing device of claim 10, wherein the input processor includes a data delay register that delays the input packet data before the input processor writes data to a packet buffer.

41. (new) The input processing device of claim 10, wherein the input processor includes a host processor interface.

42. (new) The input processing device of claim 10, wherein the input processor checks a length of each packet of said packet data received and discards packets of incorrect length.

43. (new) The input processing device of claim 41, wherein, if the input processor discards a packet of incorrect length, an error bit is set that is readable by a host processor and indicates that a packet of incorrect length was discarded.

44. (new) The input processing device of claim 10, wherein said packet identifier table lists packet identifiers for packets of data which are to be given priority and be processed before other, non-priority packets of data.

45. (new) The input processing device of claim 10, wherein the input processor accepts or discards input packet data using said packet identifier table.